AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 5, beginning at line 3, with the following amended paragraph:

> The output of the high-speed register 115, conveyed on node 116, is a single-ended digital signal. Multiple clock-phase generator 117 generates the 620 MHz clock used as the sampling clock for the high-speed register 115. The multiple clock-phase generator 117 outputs a 620 MHz clock whose phase is controlled by the phase selector signal 119 supplied from the digital control block 111. The high speed ~~register 116~~register 115 feeds *the* single-ended digital signal on node 116 to two distinct blocks, a decimator 121 and a subsampler 123.

Please replace the paragraph on page 7, beginning at line 12, with the following amended paragraph:

> Because the number of 1s and 0s may not be even and because of the possibility of long stretches of transitionless bits, it may be important to check for the signal strength for both 1s and 0's. In one embodiment, the calibration step for 0s is performed in 207 after switching the input threshold levels (thold and tholdb) provided by ~~multiplexer 103~~multiplexer 107. Once the calibration is complete in 207, the system samples a predetermined number of data bits and provides an indication of how many of the data bits have a signal strength magnitude greater than the LOS threshold (calibrated for 0s). Note that an inversion is provided in the high speed register path when sampling 0s.

Please replace the paragraph beginning on page 15, beginning at line 26, with the following amended paragraph:

> Fig. 9 illustrates the use of the digital hysteresis mode. When the LOS assert threshold is set below 10mV, the hysteresis is static at 5mV above the programmed value. Thus, as shown in ~~Fig. 10~~Fig. 9, for

program values of 6mv to 10mV, the LOS deassert level ranges from 11mV to 15mV to provide the 5mV of hysteresis. For assert values above 10mV, the hysteresis is 3 dB above the assert level. The digital hysteresis is generated by adding a digital value corresponding to 5mV to the digital threshold representation and supplying the biased-up digital threshold representation to DAC 409 on node 127. In one embodiment, the digital hysteresis is added, if required, at the end of the calibration routine.